ABSTRACT OF THE DISCLOSURE

An improved method and apparatus for reloading frames in which errors are detected during the Programmable Logic Device configuration. A configuration data frame for a FPGA is loaded to the Frame register of the FPGA and also to an error detection circuit which detects errors with the loaded frame. An error counter value is maintained by the apparatus and is incremented each time an error with a frame is detected. The incremented value is compared by a Comparator circuit with a pre-determined threshold value 'n'. If a match is found then the configuration process is aborted, else the data frame is reloaded in the configuration memory, transferred again to the frame register and rechecked for errors. If no error is detected with the reloaded frame, the error counter value is reset and the next frame is loaded until the FPGA configuration process is over.